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Implementation of an Efficient Ripple Carry Adder by Low Power Techniques for Ultra Applications

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ABSTRACT
The main goal of this paper is to provide new low power solutions for very large scale integration. Designers especially focus on the reduction of the power dissipation which shows increasing growth with the scaling down of the technologies. In this paper various technologies at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architecture and system levels. Previous technologies are summarized and compared with our new approach is presented in this paper.

The main objective of this project is the reduction of power dissipation by eliminating the PMOS tree and also by utilizing energy stored at the output can be retrieved by the reversing the current source direction discharging process instead of dissipation in NMOS network with SDCVSL, ADIABATIC LOGIC. It also increases the performance of circuits.

Here for this project, I am using MICRO WINDOW TOOL. By using this tool we can develop schematic for all above techniques and also find out the power dissipation.

Key words: Low power, CMOS, SDCVSL, Adiabatic logic.

I. INTRODUCTION:

Much of the research efforts of the past years in the area of digital electronics has been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters.

The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. In this chapter, the proper circuit style and methodology is considered. Since, most digital

Circuitry is composed of simple and/or complex gates, we study the best way to implement adders in order to achieve low power dissipation and high speed.

Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation. A review of the existing CMOS circuit design styles is given, describing their advantages and their limitations. Furthermore, a four-bit ripple carry adder for use as a benchmark circuit was designed in a full-custom manner by using the different design styles, and detailed transistor-level simulations using HSPICE [2] were performed. Also, various designs and implementations of four multipliers are analysed in the terms of delay and power consumption. Two ways of power measurements are used.

In this chapter we study two different CMOS logic styles, they are

i. STATIC DIFFERENTIAL CASCODE VOLTAGE SWITCH(SDCVSL)

ii. ADIABATIC LOGIC

Here we are comparing the parameters like power, delay and area of the above mentioned techniques with the CONVENTIONAL CMOS technique.

II. Power and Delay in Conventional CMOS Circuits:

Since the objective is to investigate the tradeoffs that are possible at the circuit level in order to reduce power dissipation while maintaining the overall system throughput, we must first study the parameters that affect the power dissipation and the speed of a circuit. It is well known that one of the major advantage of CMOS circuits over single polarity MOS circuits, is that the static power dissipation is very small and limited to leakage.

However, in some cases such as bias circuitry and pseudo-nMOS logic, static power is dissipated. Considering that in CMOS circuits the leakage current between the diffusion regions and the substrate is negligible, the two major sources of power dissipation are the switching and the short-circuit power dissipation

$$P = p_f \, C_L \, V_{dd}^2 \, f \quad + \quad I_{sc} \, V_{dd},$$

Where p_f f is the node transition activity factor, C_L is the load capacitance, V_{dd} is the supply voltage, f f is the switching frequency, I_{sc} is the current which arises when a direct path from power supply to ground is caused, for a short period of time during low to high or high to low node transitions . The switching component of power arises when energy is drawn from the power supply to charge parasitic capacitors. It is the dominant power component in a well designed circuit and it can be lowered by reducing one or more of pf , CL, Vdd and f, while retaining the required speed and functionality.

Even though the exact analysis of circuit delay is quite complex, a simple first-order derivation can be used in order to show its dependency of the circuit parameters

$$T_d \quad \propto \quad \frac{C_L \, V_{dd}}{K \ (V_{dd} - V_{th})^{\alpha}},$$

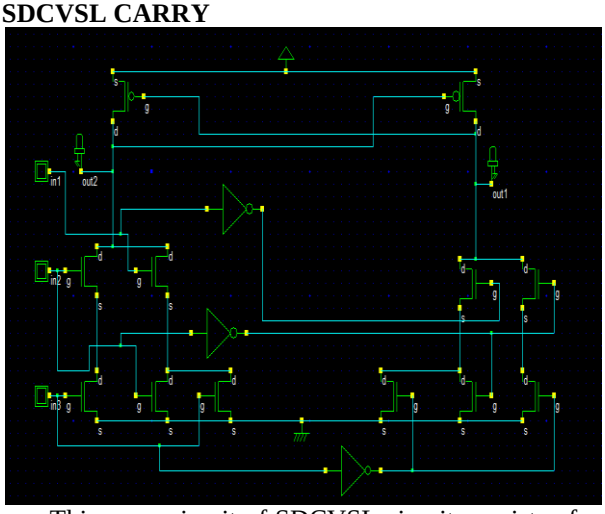
where K depends on the transistors aspe
eters, V_{TH} is the transistor threshold vo
index which varies between 1 and 2 (α

III. Static Differential Cascode Voltage Switch :

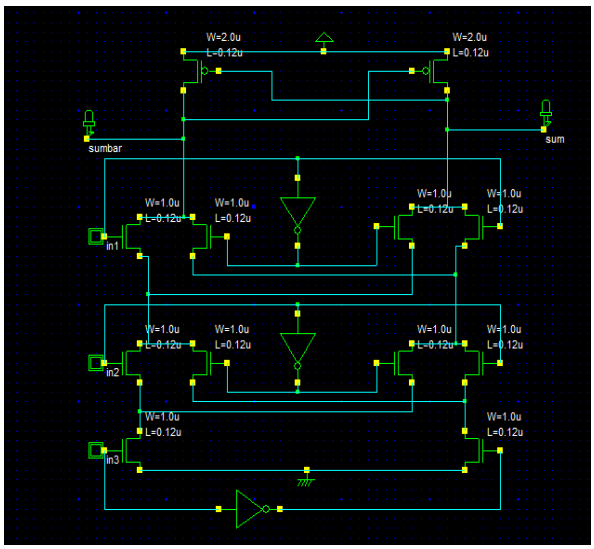
Static DCVSL is a differential style of logic requiring both true and complementary Signals to be routed to gates. Figure 5.4 shows the circuit diagram of the static DCVSL full adder. Two complementary NMOSFET switching trees are constructed to a pair of cross-coupled PMOSFET transistors.

Depending on the differential inputs one of the outputs is pulled down by the corresponding NMOSFET network. The differential output is then latched by the cross-coupled PMOSFET transistors. Since the inputs drive only the NMOSFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic.

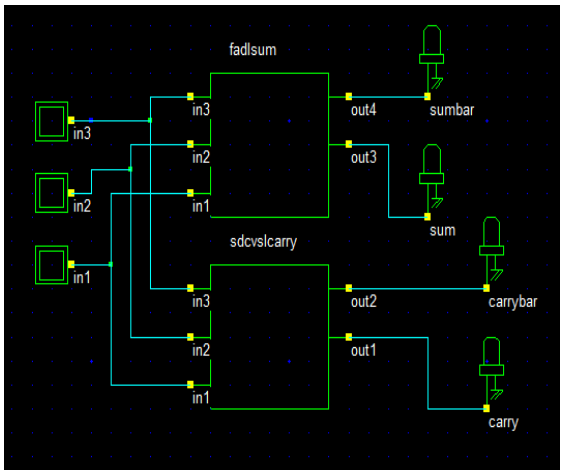
SDCVSL CARRY



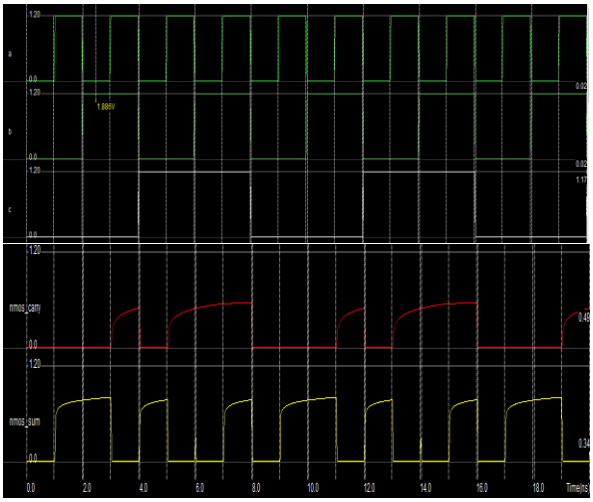
This carry circuit of SDCVSL circuit consists of 12 transistors with 3 inputs.



SDCVSL SUM



SDCVSL FULL ADDER



IV. ADIABATIC LOGIC:

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value.

1. Conventional Switching

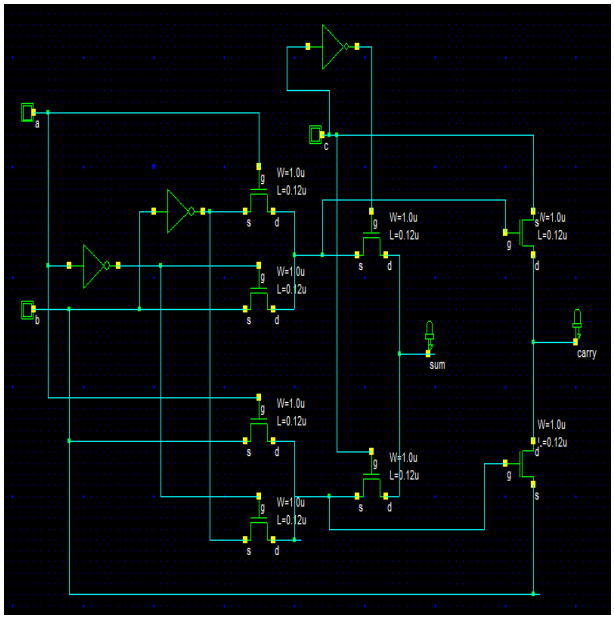
There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance.

2. Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from time varying voltage source or constant current source.

In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system. There are two types of energy loss in quasi-adiabatic circuits, adiabatic loss and nonadiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock.

If any voltage difference between the two terminals of a switch exists when it is turned on, non-adiabatic loss occurs. The non-adiabatic loss, which is independent of the frequency of the power-clock, is proportional to the node capacitance and the square of the voltage difference. Several quasi-adiabatic logic architectures have been reported, such as ECRL, 2N-2N-2P, PFAL.



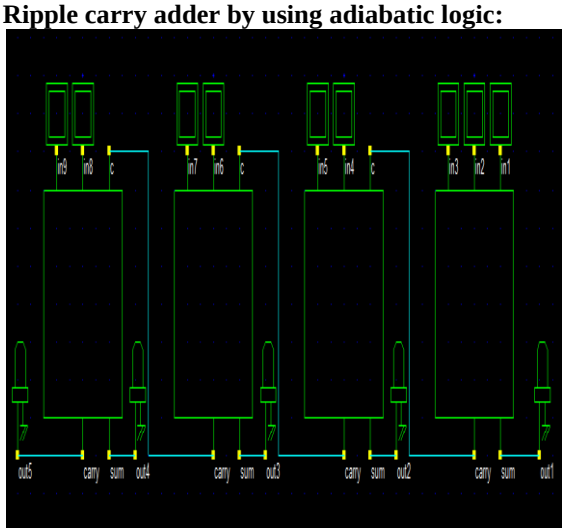
ADIABATIC FULL ADDER

USING PASS TRANSISTOR

Technique	power	Area	Delay
CMOS	16.969uw	62*12um	18ps
SDCVSL	0.164mw	42*13um	0.94ns
Adiabatic	7.037uw	16*13um	8.88ns

From the above analysis, we came to know that adiabatic logic is the best technique. So we design ripple carry adder using the adiabatic technique because it consumes less power.

Ripple carry adder by using adiabatic logic:



Above ripple carry adder is designed by using adiabatic full adder. It consists of four full adders. This ripple carry adder consumes less power as adiabatic logic technique is the efficient in

consuming less power and reducing power dissipation.

V. CONCLUSION

In this chapter, the most common kinds of adders have been characterized in terms of power, using either a traditional low-level design flow paradigm, which is rather tedious and incompatible with modern design flows, but provides the most accurate results, or a high-level design flow paradigm, which is commonly used.

In this paper we compared the performance of SDCVSL and adiabatic logic adder circuits with traditional CMOS adder circuits. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

A four-bit ripple carry adder was designed using adiabatic logic here is used as the benchmark circuit. All the circuits have been designed in a full-custom manner.

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